Please add the following new claims.

6. (New) Scan test circuitry in an integrated circuit having a logic block including elements capable of disturbing a scan test, comprising:

a plurality of flip-flops operable as a register in a scan test mode;

inhibiting circuits for inhibiting each of the disturbing elements of the logic block from disturbing a scan test; and

a controller for individually controlling each of the inhibiting circuits during a scan test.

A3

7. (New) Scan test circuitry as defined in claim 6, wherein the controller is configured to load into the flip-flops, with all disturbing elements inhibited, a test vector for testing a first disturbing element and, subsequently, to enable the first disturbing element and to observe operation of the logic block in response to the test vector.

8. (New) Scan test circuitry as defined in claim 7, wherein the controller is configured to scan test the first disturbing element in an active state in response to a first test vector and to scan test the first disturbing element in an inactive state in response to a second test vector.

9. (New) Scan test circuitry as defined in claim 6, wherein the controller is configured to individually scan test each of the disturbing elements in active and inactive states.

10. (New) Scan test circuitry as defined in claim 6, wherein the controller is configured to:

load into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enable the first disturbing element with all other disturbing elements inhibited;

observe operation of the logic block in response to the first test vector;

load into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enable the first disturbing element with all other disturbing elements inhibited; and

observe operation of the logic block in response to the second test vector.

11. (New) Scan test circuitry as defined in claim 6, wherein the controller is further configured to perform a scan test with all disturbing elements inhibited by the respective inhibiting circuits.

12. (New) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a clock signal supplied to at least one of the flip-flops.

13. (New) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a reset signal supplied to at least one of the flip-flops.

A3

14. (New) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one input from the scan test circuitry to the logic block.

15. (New) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one output of the logic block to the scan test circuitry.

16. (New) In an integrated circuit having a plurality of flip-flops operable as a register in a scan test mode and a logic block including elements capable of disturbing a scan test, a scan test method comprising:

(a) inhibiting all of the disturbing elements except a selected disturbing element;

(b) performing a scan test of the selected disturbing element;

(c) repeating steps (a) and (b) for each disturbing element in the logic block; and

(d) performing a scan test of the logic block with all of the disturbing elements inhibited.

17. (New) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises loading into the flip-flops a first test vector for scan

testing the selected disturbing element in an active state and observing operation of the logic block in response to the first test vector.

18. (New) A scan test method as defined in claim 17, wherein performing a scan test of the selected disturbing element further comprises loading into the flip-flops a second test vector for scan testing the selected disturbing element in an inactive state and observing operation of the logic block in response to the second test vector.

19. (New) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects a clock signal supplied to at least one of the flip-flops.

A3

20. (New) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects a reset signal supplied to at least one of the flip-flops.

21. (New) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects a reset signal supplied to at least one of the flip-flops.

22. (New) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects an input to the logic block from at least one of the flip-flops.

23. (New) scan test A method as defined in claim 16, wherein inhibiting all of the disturbing elements except a selected disturbing element comprises inhibiting at least one disturbing element that affects an output of the logic block to at least one of the flip-flops.

24. (New) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises inhibiting the selected disturbing element to load a test

vector into the flip-flops and enabling the selected disturbing element to observe operation of the logic block in response to the test vector.

25. (New) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises scan testing the selected disturbing element in active and inactive states.

A3 Cont.

26. (New) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises:

loading into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enabling the first disturbing element with all other disturbing elements inhibited;

observing operation of the logic block in response to the first test vector;

loading into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enabling the first disturbing element with all other disturbing elements inhibited; and

observing operation of the logic block in response to the second test vector.

REMARKS

In this Preliminary Amendment, claims 2 and 5 have been amended to correct minor errors. Claims 6-26 have been added. No new matter has been introduced.

Claims 1-26 are now pending in the application. The application is now ready for examination on the merits.